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transmitted to the United States Patent and Trademark Office,
Examiner Paul E. Brock II at fax number 1-703-872-9318 on

October 14, 2002

PATENT
Attorney Docket No.: 015114-047930US
Client Ref. No.: A293-D1

TOWNSEND and TOWNSEND and CREW LLP

By: T. Matthews

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Raminda U. Madurawe et al.

Application No.: 09/606,252

Filed: June 28, 2000

For: HIGH VOLTAGE MOS DEVICES
WITH HIGH GATED-DIODE
BREAKDOWN VOLTAGE AND
PUNCH-THROUGH VOLTAGE

Examiner: Paul E. Brock II

Art Unit: 2815

AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

FAX COPY RECEIVED

OCT 15 2002

TECHNOLOGY CENTER 2800

Sir:

In response to the office action mailed April 15, 2002, please amend the
above-identified application as follows:

IN THE CLAIMS:

✓
Please cancel claims 21-26, 39, and 41 without prejudice. Please amend
claims 27, 31, and 38 as indicated. Please add new claims 42-44.

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- 1 27. (Amended) A method of fabricating a transistor in an integrated
 - 2 circuit device comprising:
 - 3 providing a semiconductor substrate;
 - 4 forming a gate oxide on the semiconductor substrate;
 - 5 forming a gate on the gate oxide;